

Spread Spectrum Clock Generator Ultra Low Power Mobile EMI Reduction IC SSDCP3138AF

DESCRIPTION

The SSDCP3138AF is a versatile 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) clock and data source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The SSDCP3138AF allows significant system cost savings by reducing the number of circuit board layers ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.

The SSDCP3138AF family of mobile active EMI management ICs are unique in their design by elimiating the use of conventional PLLs. This allows operation on aperiodic as well periodic signals. The peak energy is distributed over a wider and controlled energy band thereby significantly lowering system

■ FEATURE

- FCC approved method of EMI attenuation.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input / Output frequency

 VDD 1.65V-3.6V 10 MHz to 60 MHz
- Multiple Deviation Selections
- (Refer product table)
- Power save mode
- 8-pin TDFN package
- Operating Temperature $~0\ensuremath{\,^\circ C}$ to $70\ensuremath{\,^\circ C}$

EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is known as "Spread Spectrum" or active EMI management.

3138 has an input frequency range of 10 MHZ to 60 MHz over a wide voltage range of 1.65V to 3.6V and generates a 1x spread spectrum coutput. The device can be placed in "power save mode" by setting the PDB pin to GND where in it draws typically 0.1uA and also stes the MODOUT pin to a High-Z state. The device has to "deviation control pins" SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well in system design.

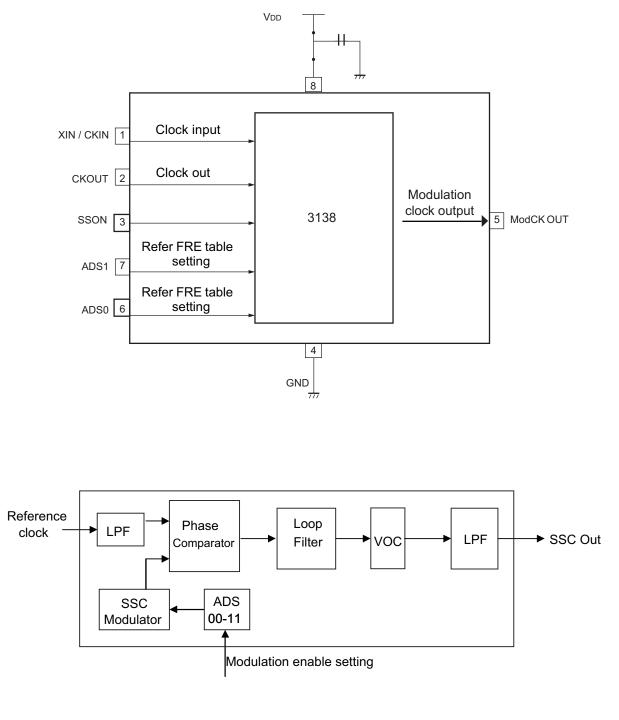
Application

3138 is targeted for consumer electronics application such as MFP, STB, DSC, MID, HDMI,LCD panel Camcorder,and other timing sensitive analog video imaging applications

Applications of HDMI, RJ45 port has good compatibility



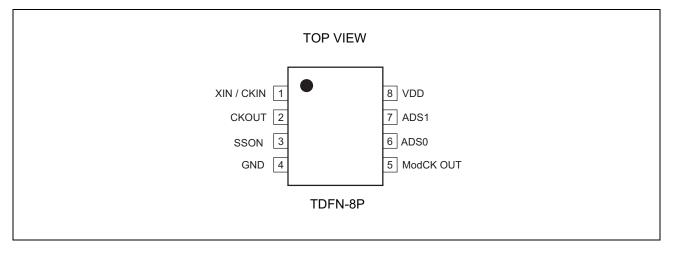
BLOCK DIAGRAM



SSDCP3138AF block



PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
XIN / CKIN	Ι	1	Clock input pin (or External reference clock input).
СКОИТ	0	2	Crystal connection(external reference, this pin should be left open)
SSON	Ι	3	ModCK OUT ON/OFF 1=ON 0=OFF
GND		4	GND pin
ModCK OUT	0	5	Modulation clock output
ADS	Ι	6	Analog Deviation Selection(refer Functionality Table)
ADS	Ι	7	Analog Deviation Selection(refer Functionality Table)
VDD		8	Power supply voltage pin

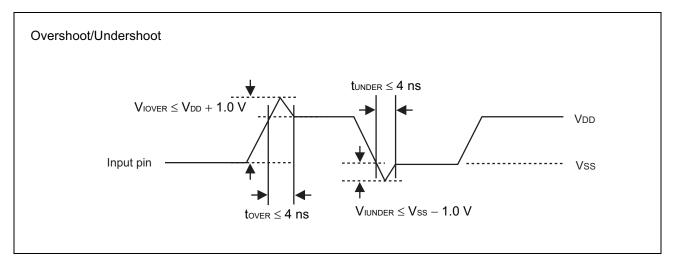


Parameter	Symbol	Rat	Unit		
Parameter	Symbol	Min	Мах		
Power supply voltage*	Vdd	- 0.5	+ 4.5	V	
Input voltage*	Vı	Vss – 0.5	V _{DD} + 0.5	V	
Output voltage*	Vo	Vss - 0.5	V _{DD} + 0.5	V	
Storage temperature	Ts⊤	– 55	+ 125	°C	
Operation junction temperature	TJ	0	+70	°C	
Output current	lo	2	4	mA	
Overshoot	VIOVER		V_{DD} + 1.0 (tover \leq 4ns)	V	
Undershoot	VIUNDER	$V_{\text{SS}} - 1.0 \text{ (tunder} \leq 4 \text{ns})$	—	V	

ABSOLUTE MAXIMUM RATINGS

* : The parameter is based on $V_{\text{SS}} = 0.0 \text{ V}.$

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.





ELECTRICAL CHARACTERISTICS

DC Characteristics

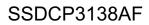
$(Ta = 0 \ ^{\circ}C \text{ to } +70 \ ^{\circ}C, V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}, \text{ V}_{SS} = 0.0 \text{ V})$										
Devementer	Symbol	Dim	Conditions			11				
Parameter	Symbol	Pin	Conditions	Min	Max	Unit				
Output voltage	Vон	СКОИТ	"H" level output Іон = - 4 mA	0.66Vdd		Vdd	V			
Output voltage	Vol	СКОИТ	"L" level output Io∟ = 4 mA	Vss	_	0.33Vdd	V			
Output impedance	Zo	CKOUT	10 MHz to 60 MHz		30		Ω			
Input capacitance	Cin	CKIN,	$ \begin{array}{l} Ta = \ + \ 25 \ ^{\circ}C, \\ V_{\text{DD}} = V_{\text{I}} = 0.0 \ V, \\ f = 1 \ MHz \end{array} $		_	16	pF			
Load capacitance	C∟	CKOUT	10 MHz to 60 MHz			10	pF			
Power supply current	lcc	Vdd	No load capacitance at 27 MHz		3.0	4	mA			
Power down current	lpd	Vdd	Input clock stopping		4		μA			

• AC Characteristics

(Ta = 0 °C to + 70 °C, V_{DD} = 3.3 V \pm 0.3 V, Vss = 0.0 V)

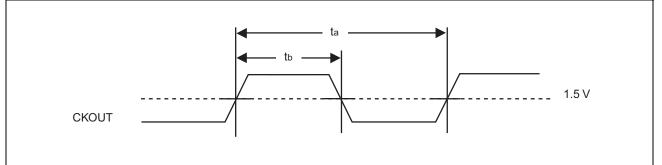
Parameter	Symbol	Pin	Conditions		Value		Unit	
Parameter	Symbol	FIII	Conditions	Min	Тур Мах			
Input frequency	fin	CKIN	_	10.0	_	60	MHz	
Output frequency	fouт	CKOUT	_	10.0	_	60	MHz	
Output slew rate	SR	СКОИТ	Load capacitance 15 pF 0.4 V to 2.4 V	0.4		4.0	V/ns	
Output clock duty cycle	tDCC	CKOUT	1.5 V	45	_	55	%	
Output Rise Time			between 20% to 80%		0.9		nS	
Output Fall Time			between 80% to 20%		0.9		nS	
Cycle-cycle jitter	tuc	CKOUT	No load capacitance, Ta = $+25 \text{ °C}$, V _{DD} = 3.3 V	_		40	ps-rms	

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

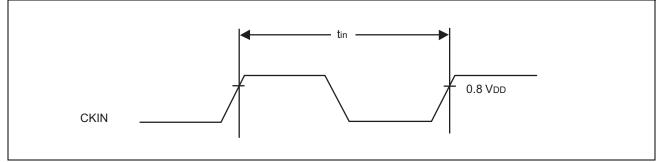




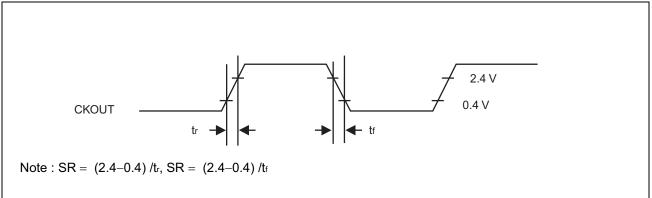
OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



■ INPUT FREQUENCY (fin = 1/tin)



OUTPUT SLEW RATE (SR)





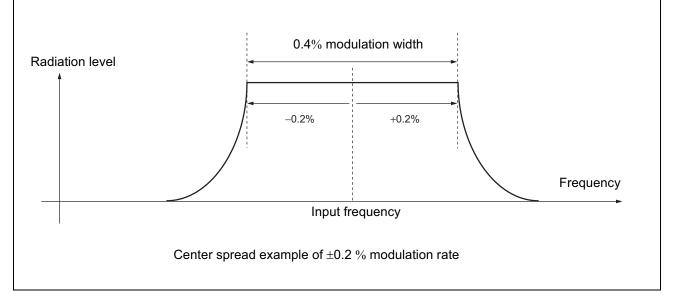
Functional Table

Vdd(V)	Freq.	Freq.				Dev	viation (%)			
	Range	(MHz)	SS1	SS0	SS1	SS0	SS1	SS0	SS1	SS0
	(MHz)		0	0	0	1	1	0	1	1
1.8		12	±0	±0.05		±0.10		±0.14		.18
1.8	10~33	24	±0	±0.06		±0.12		±0.15		-
1.8	27		±0.07		±0.13		±0.13		-	
1.8		32	±0	±0.08		-		-		-
3.3		12	±0	.03	±0.06		±0.09		±0.11	
3.3	10.00	24	±0	±0.05		±0.10		±0.13		.16
3.3	10~60	27	±0	.06	±0	.12	±0	.15	±0	.17
3.3		32	±0	.06	±0	±0.12		±0.15		.17

Note: Frequency deviation can vary over voltage and temperature by 5%

• Center spread

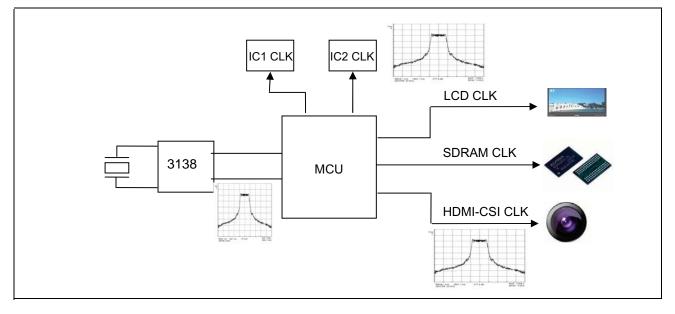
Spectrum is spread (modulated) by centering on the input frequency.



SSDCP3138AF

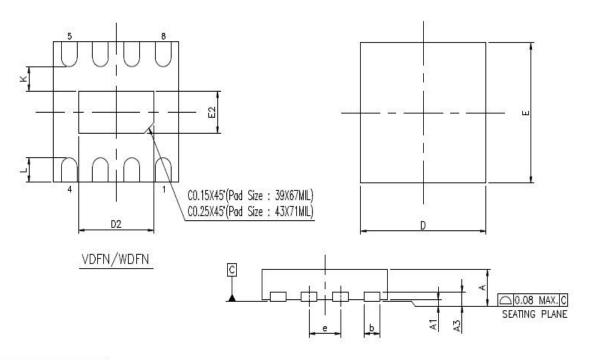


• Diagram of CLK spread





TDFN-2×2-8L



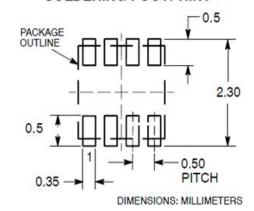
JEDEC OUTLINE	M0-229								
PKG CODE	WD	WDFN(X208)							
SYMBOLS	MIN.	NOM.	MAX.						
Α	0.70	0.75	0.80						
A1	0.00	0.02	0.05						
A3	0.203 REF.								
b	0.20	.20 0.25							
D	2	.00 BS	С						
E	2	.00 BS	С						
e	0	.50 BS	SC						
K	0.20	-	-						

NOTES	5 :

- 1. ALL DIMENSIONS ARE IN MILLIMETERS.
- 2. DIMENSION & APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION & SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
- 3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

6	2			D2		-	E2			LL		LEAD FINISH			inni	woou	UDEN	TOEN	TOEN
	PAD	SIZE	MIN.	NOM.	MAX,	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	JEDEC CODE	VUTIN	WUTH	OUTN	OPTION 1	
A	39*X67	7* ML	1.15	1.20	1.25	0.60	0.65	0.70	0.20	0.35	0.45	V	Х	N/A	٧	٧	_		_

RECOMMENDED SOLDERING FOOTPRINT*



▲ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.



SSDCP3138AF

Ordering Code

Part Number	Temperature	
SSDCP3138AF-08-CT	8- pin 2-mm TDFN COL - TAPE & REEL, Green	0°C to +70 °C

Device Ordering Information

