Spread Spectrum Clock Generator
Ultra Low Power Mobile EMI Reduction IC
SSDCA3138AF

■ DESCRIPTION

The SSDCA3138AF is a versatile 1x spread spectrum frequency modulator designed to reduce electromagnetic interference (EMI) clock and data source, allowing system wide reduction of EMI of down stream clock and data dependent signals. The SSDCA3138AF allows significant system cost savings by reducing the number of circuit board layers, ferrite beads, shielding and other passive components that are traditionally required to pass EMI regulations.
The SSDCA3138AF family of mobile active EMI management ICs are unique in their design by elimiating the use of conventional PLLs. This allows operation on aperiodic as well periodic signals. The peak energy is distributed over a wider and controlled energy band thereby significantly lowering system EMI compared to the typical narrow band signal produced by oscillators and most frequency generators. Lowering EMI by increasing a signal's bandwidth is known as "Spread Spectrum" or active EMI management.

3138 has an input frequency range of 10 MHZ to 60 MHz over a wide voltage range of 1.65V to 3.6V and generates a 1x spread spectrum coutput. The device can be placed in "power save mode" by setting the PDB pin to GND where in it draws typically 0.1uA and also stes the MODOUT pin to a High-Z state. The device has to "deviation control pins" SS1 and SS0 to allow flexibility and optimization of both EMI compliance as well in system design.

■ FEATURE

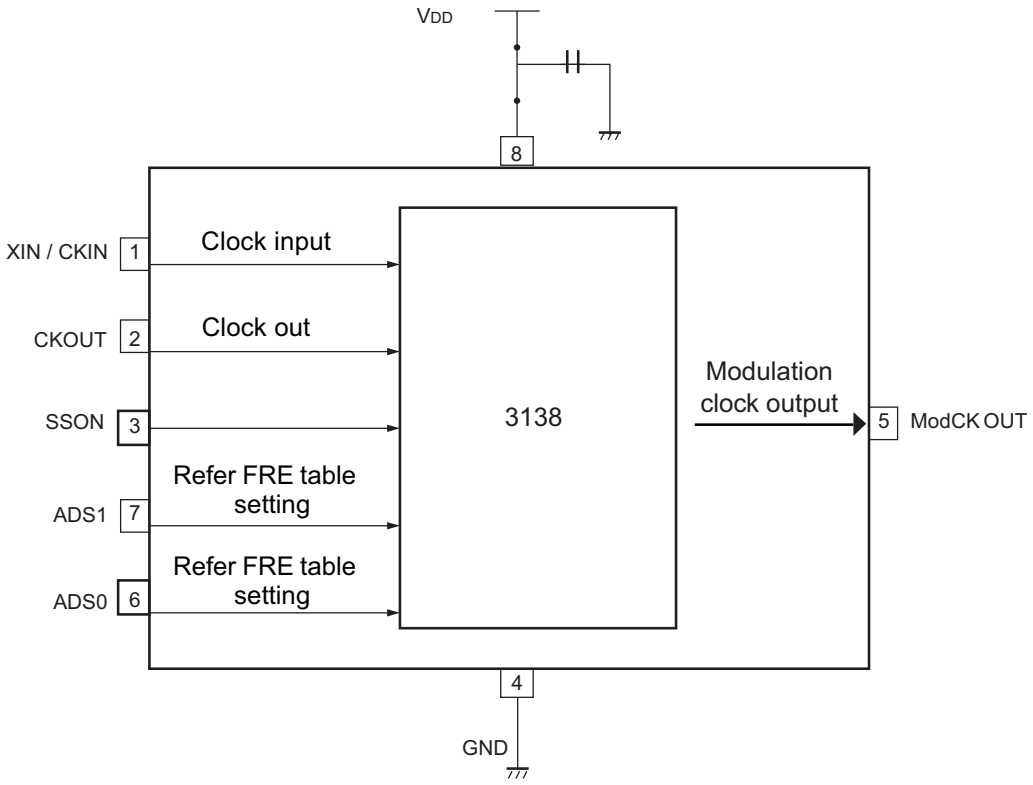
- FCC approved method of EMI attenuation.
- Generates a 1X low EMI spread spectrum clock of the input frequency.
- Input / Output frequency
  - VDD 1.65V-3.6V 10 MHz to 60 MHz
- Multiple Deviation Selections
- (Refer product table)
- Power save mode
- 8-pin TDFN package
- Operating Temperature -40℃ to 125℃

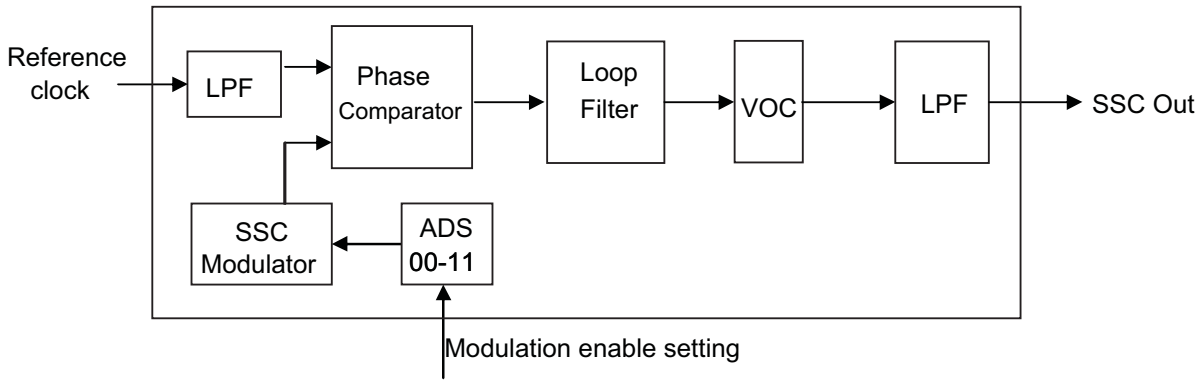
■ Application

3138 is targeted for consumer electronics application such as MFP, STB, DSC, MID, HDMI,LCD panel Camcorder,and other timing sensitive analog video imaging applications

Applications of HDMI, RJ45 port has good compatibility

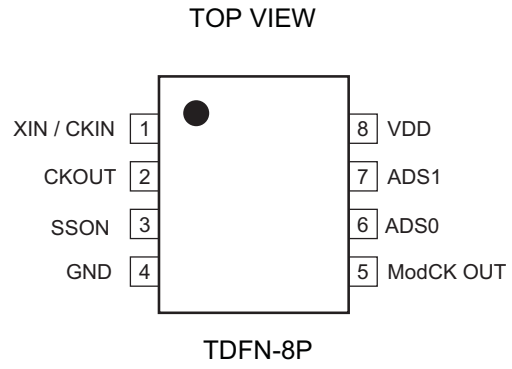
■ BLOCK DIAGRAM





SSDCA3138AF block

■ PIN ASSIGNMENT



■ PIN DESCRIPTION

Pin name	I/O	Pin no.	Description
XIN / CKIN	I	1	Clock input pin (or External reference clock input).
CKOUT	O	2	Crystal connection(external reference, this pin should be left open)
SSON	I	3	ModCK OUT ON/OFF 1=ON 0=OFF
GND	---	4	GND pin
ModCK OUT	O	5	Modulation clock output
ADS	I	6	Analog Deviation Selection(refer Functionality Table)
ADS	I	7	Analog Deviation Selection(refer Functionality Table)
VDD	---	8	Power supply voltage pin

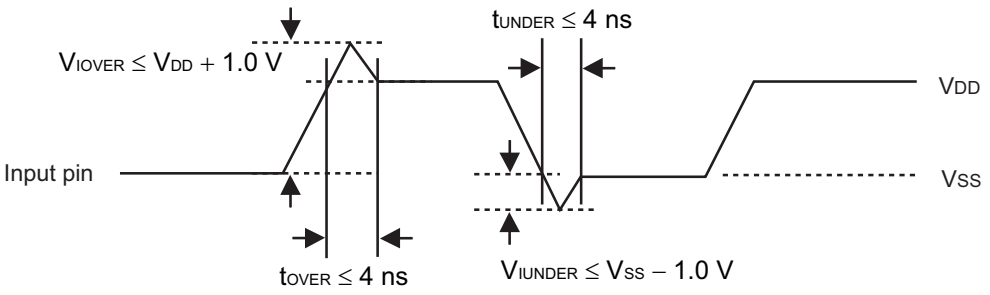
■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	V_{DD}	− 0.5	+ 4.5	V
Input voltage*	V_I	V_{SS} − 0.5	V_{DD} + 0.5	V
Output voltage*	V_O	V_{SS} − 0.5	V_{DD} + 0.5	V
Storage temperature	T_{ST}	− 55	+ 150	°C
Operation junction temperature	T_J	-40	+125	°C
Output current	I_O	2	4	mA
Overshoot	V_{IOVER}	—	V_{DD} + 1.0 (t_{OVER} ≤ 4ns)	V
Undershoot	V_{IUNDER}	V_{SS} − 1.0 (t_{UNDER} ≤ 4 ns)	—	V

* : The parameter is based on V_{SS} = 0.0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Overshoot/Undershoot



■ ELECTRICAL CHARACTERISTICS

• DC Characteristics

($Ta = -40\,°C$ to $+125°C$, $V_{DD} = 3.3\ V \pm 0.3\ V$, $V_{SS} = 0.0\ V$)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Output voltage	V_{OH}	CKOUT	"H" level output $I_{OH} = -4$ mA	$0.66V_{DD}$	—	V_{DD}	V
	V_{OL}	CKOUT	"L" level output $I_{OL} = 4$ mA	V_{SS}	—	$0.33V_{DD}$	V
Output impedance	Z_O	CKOUT	10 MHz to 60 MHz	—	30	—	Ω
Input capacitance	C_{IN}	CKIN,	Ta = + 25 °C, $V_{DD} = V_I = 0.0$ V, f = 1 MHz	—	—	16	pF
Load capacitance	C_L	CKOUT	10 MHz to 60 MHz	—	—	10	pF
Power supply current	I_{CC}	V_{DD}	No load capacitance at 27 MHz	—	3.0	4	mA
Power down current	Ipd	V_{DD}	Input clock stopping	—	4	—	μA

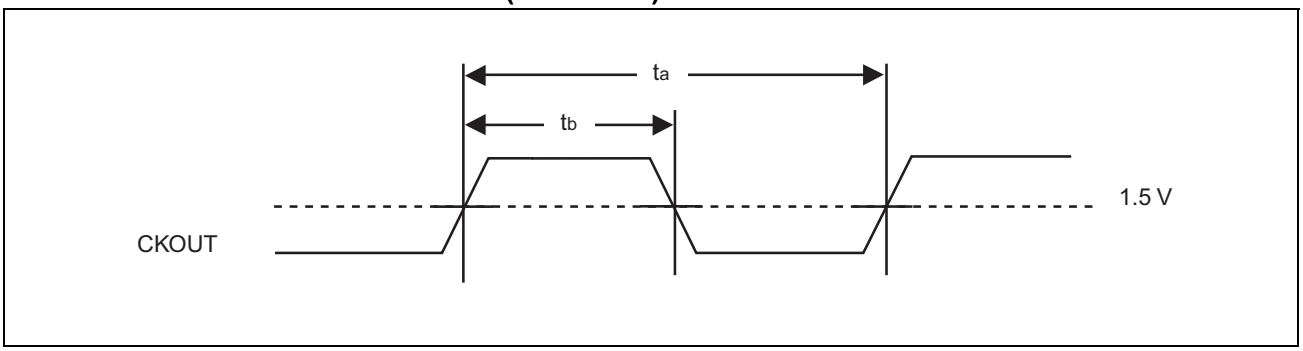
• AC Characteristics

($Ta = -40°C$ to $+125°C$, $V_{DD} = 3.3\ V \pm 0.3\ V$, $V_{SS} = 0.0\ V$)

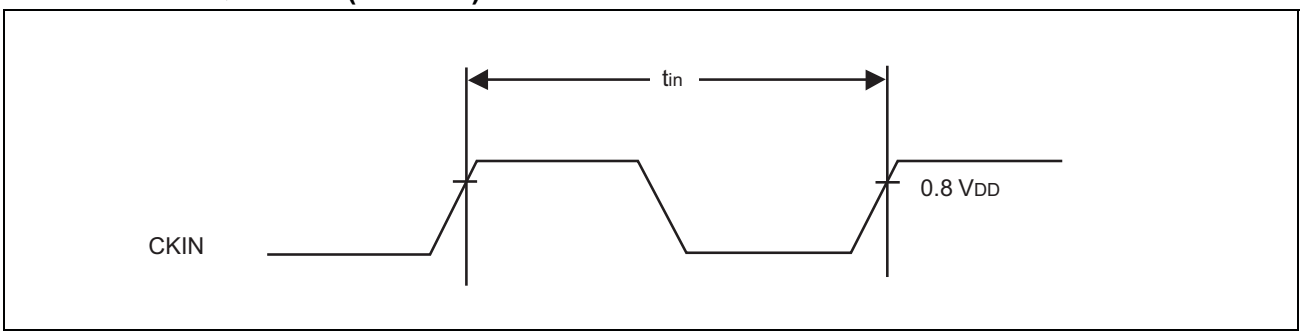
Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Input frequency	f_{in}	CKIN	—	10.0	—	60	MHz
Output frequency	f_{OUT}	CKOUT	—	10.0	—	60	MHz
Output slew rate	SR	CKOUT	Load capacitance 15 pF 0.4 V to 2.4 V	0.4	—	4.0	V/ns
Output clock duty cycle	t_{DCC}	CKOUT	1.5 V	45	—	55	%
Output Rise Time			between 20% to 80%		0.9		nS
Output Fall Time			between 80% to 20%		0.9		nS
Cycle-cycle jitter	t_{JC}	CKOUT	No load capacitance, Ta = + 25 °C, $V_{DD} = 3.3$ V	—	—	40	ps-rms

Note : The modulation clock stabilization wait time is required after the power is turned on, the IC recovers from power saving, or after ENS (modulation ON/OFF) setting is changed. For the modulation clock stabilization wait time, assign the maximum value for lock-up time.

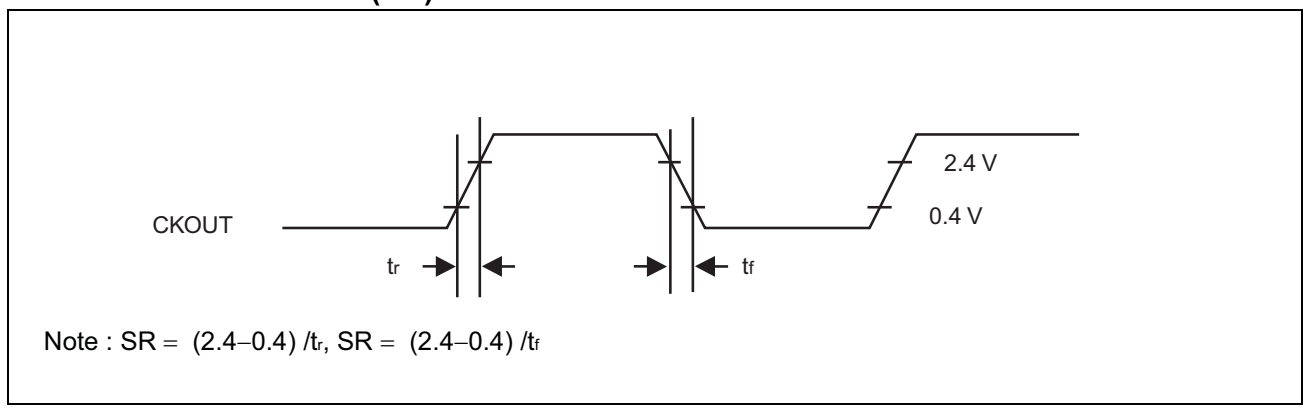
■ OUTPUT CLOCK DUTY CYCLE ($t_{DCC} = t_b/t_a$)



■ INPUT FREQUENCY ($f_{in} = 1/t_{in}$)



■ OUTPUT SLEW RATE (SR)



Note : SR = (2.4–0.4) /t_r, SR = (2.4–0.4) /t_f

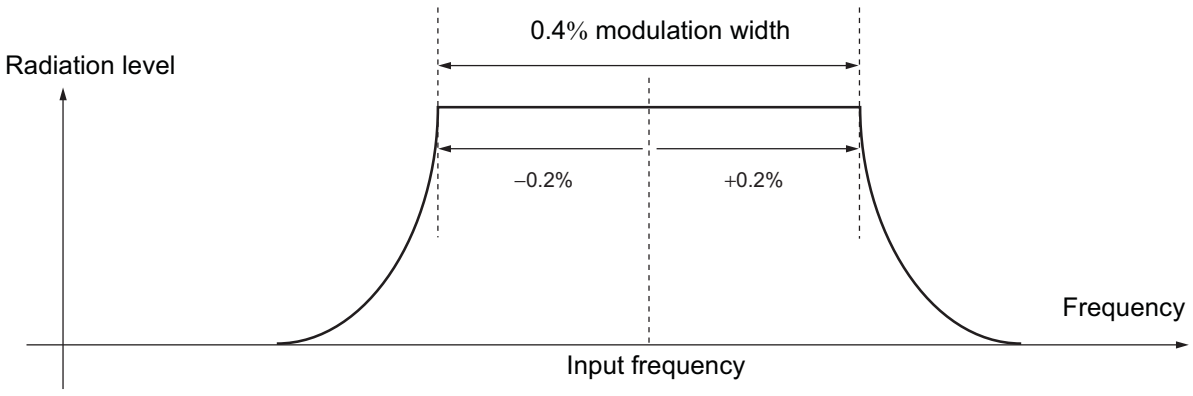
Functional Table

Vdd(V)	Freq. Range (MHz)	Freq. (MHz)	Deviation (%)							
			SS1	SS0	SS1	SS0	SS1	SS0	SS1	SS0
			0	0	0	1	1	0	1	1
1.8	10~33	12	±0.05		±0.10		±0.14		±0.18	
1.8		24	±0.06		±0.12		±0.15		-	
1.8		27	±0.07		±0.13		±0.13		-	
1.8		32	±0.08		-		-		-	
3.3	10~60	12	±0.03		±0.06		±0.09		±0.11	
3.3		24	±0.05		±0.10		±0.13		±0.16	
3.3		27	±0.06		±0.12		±0.15		±0.17	
3.3		32	±0.06		±0.12		±0.15		±0.17	

Note: Frequency deviation can vary over voltage and temperature by 5%

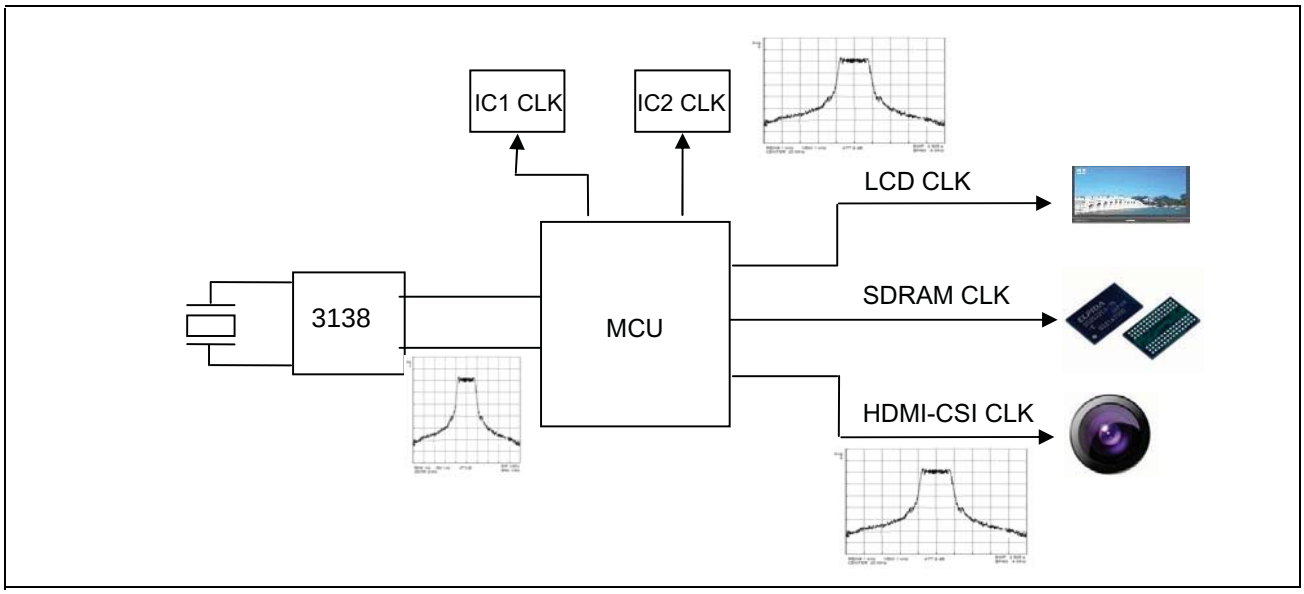
- Center spread

Spectrum is spread (modulated) by centering on the input frequency.

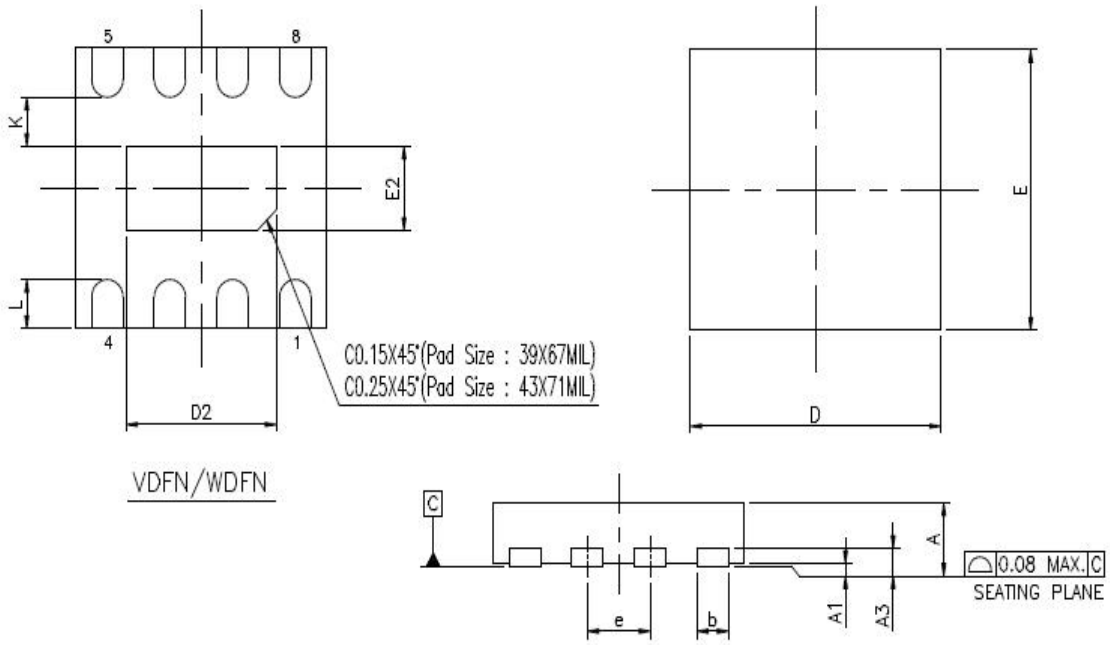


Center spread example of ±0.2 % modulation rate

• Diagram of CLK spread



TDFN-2×2-8L

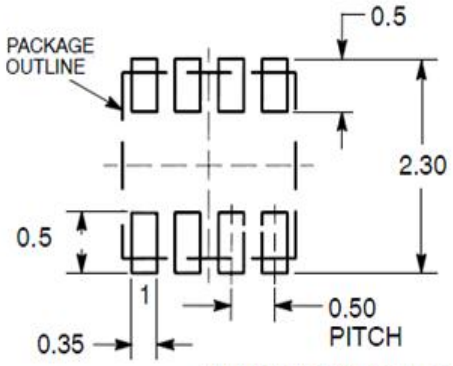


JEDEC OUTLINE	MO-229		
PKG CODE	WDFN(X208)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	2.00 BSC		
E	2.00 BSC		
e	0.50 BSC		
K	0.20	—	—

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

	D2			E2			L			LEAD FINISH		JEDEC CODE	VDFN	WDFN	UDFN	TDFN OPTION 1	TDFN OPTION 2
PAD SIZE	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF						
⚠ 39*X67* MIL	1.15	1.20	1.25	0.60	0.65	0.70	0.20	0.35	0.45	V	X	N/A	V	V	—	—	—

⚠ "*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Ordering Code

Part Number	Package	Temperature
SSDCA3138AF-08-CT	8- pin 2-mm TDFN COL - TAPE & REEL, Green	-40°C to +125°C

Device Ordering Information