

**FEATURES**

- 19MHz to 65MHz crystal input.
- Output range: 9.5MHz – 65MHz
- Selectable OE Logic (enable high or enable low).
- Available outputs: PECL, LVDS, or CMOS (High Drive (30mA) or Standard Drive (10mA) output).
- Supports 2.5V or 3.3V Power Supply.
- Available in die form.

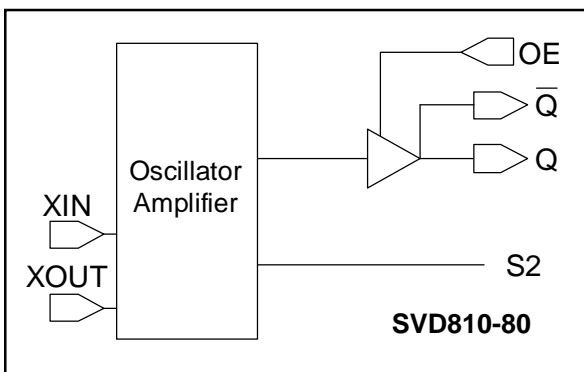
**DESCRIPTION**

The SVD810-80 is a XO IC specifically designed to work with fundamental or 3<sup>rd</sup> OT crystals between 19MHz and 65MHz. The selectable divide by two feature extends the operation range from 9.5MHz to 65MHz. It requires very low current into the crystal resulting in better overall stability. The OE logic feature allows selection of enable high or enable low. Furthermore, it provides selectable CMOS, PECL or LVDS outputs.

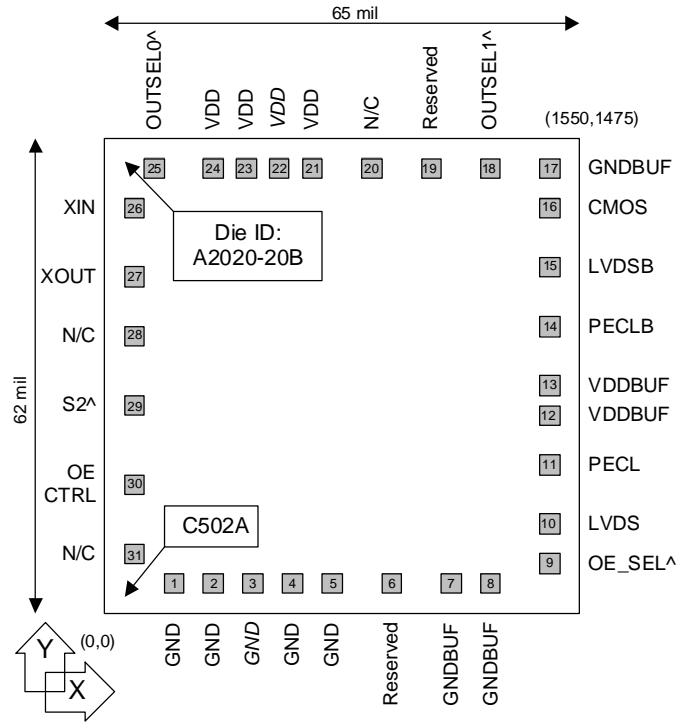
**DIE SPECIFICATIONS**

Name	Value
Size	62 x 65 mil
Reverse side	GND
Pad dimensions	80 micron x 80 micron
Thickness	10 mil

**BLOCK DIAGRAM**



**DIE CONFIGURATION**



**OUTPUT SELECTION AND ENABLE**

OUT_SEL1* (Pad 18)	OUT_SEL0* (Pad 25)	Selected Output*
0	0	High Drive CMOS
0	1	Standard CMOS
1	0	LVDS
1	1	PECL (default)

OE_SELECT (Pad 9)	OE_CTRL (Pad 30)	State
0	0	Tri-state
	1 (Default)	Output enabled
1 (Default)	0 (Default)	Output enabled
	1	Tri-state

Pads #9, #18 & #25: Bond to GND to set to "0",  
No connection results to "default" setting through internal pull-up.  
OE\_CTRL: Logical states defined by PECL levels if OE\_SELECT is "1"  
Logical states defined by CMOS levels if OE\_SELECT is "0"

**OUTPUT FREQUENCY SELECTOR**

S2	Output
0	Input/2
1(Default)*	Input

\*Internally set to 'Default' through 60KΩ pull-up resistor

## ELECTRICAL SPECIFICATIONS

### 1. Absolute Maximum Ratings

PARAMETERS	SYMBOL	MIN.	MAX.	UNITS
Supply Voltage	$V_{DD}$		4.6	V
Input Voltage, dc	$V_I$	-0.5	$V_{DD}+0.5$	V
Output Voltage, dc	$V_O$	-0.5	$V_{DD}+0.5$	V
Storage Temperature	$T_S$	-65	150	°C
Ambient Operating Temperature	$T_A$	-40	85	°C
Junction Temperature	$T_J$		125	°C
Lead Temperature (soldering, 10s)			260	°C
ESD Protection, Human Body Model			2	kV

Exposure of the device under conditions beyond the limits specified by Maximum Ratings for extended periods may cause permanent damage to the device and affect product reliability. These conditions represent a stress rating only, and functional operations of the device at these or any other conditions above the operational limits noted in this specification is not implied.

### 2. Crystal Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Crystal Resonator Frequency	$F_{XIN}$	Fundamental	19		65	MHz
Crystal Loading Rating	$C_L$ (xtal)	Die		8*		pF
Interelectrode Capacitance	$C_0$				5	pF
Recommended ESR	$R_E$	AT cut			30	$\Omega$

Note: Parameters denoted with an asterisk (\*) represent nominal characterization data and are not production tested to any specific limits.

### 3. General Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current (Loaded Outputs)	$I_{DD}$	PECL/LVDS/CMOS			100/80/40	mA
Operating Voltage	$V_{DD}$		2.25		3.63	V
Output Clock Duty Cycle		@ 50% $V_{DD}$ (CMOS) @ 1.25V (LVDS) @ $V_{DD} - 1.3V$ (PECL)	45 45 45	50 50 50	55 55 55	%
Short Circuit Current				$\pm 50$		mA

#### 4. Jitter Specifications

PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Period jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 10,000 cycles		2.3		ps
Period jitter peak-to-peak at 27MHz			18.5	20	
Accumulated jitter RMS at 27MHz	With capacitive decoupling between VDD and GND. Over 1,000,000 cycles.		2.3		ps
Accumulated jitter peak-to-peak at 27MHz			24	25	
Random Jitter	"RJ" measured on Wavecrest SIA 3000		2.3		ps

Measured on Wavecrest SIA 3000

#### 5. CMOS Output Electrical Specifications

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output drive current (High Drive)	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	30			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	30			mA
Output drive current (Standard Drive)	I <sub>OH</sub>	V <sub>OH</sub> = V <sub>DD</sub> -0.4V, V <sub>DD</sub> =3.3V	10			mA
	I <sub>OL</sub>	V <sub>OL</sub> = 0.4V, V <sub>DD</sub> = 3.3V	10			mA
Output Clock Rise/Fall Time (Standard Drive)		0.3V ~ 3.0V with 15 pF load		2.4		ns
Output Clock Rise/Fall Time (High Drive)		0.3V ~ 3.0V with 15 pF load		1.2		

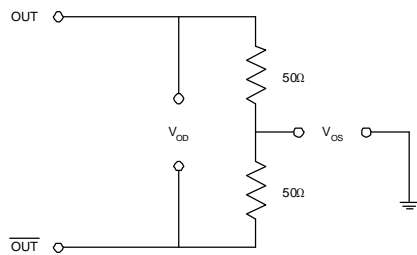
#### 6. LVDS Electrical Characteristics

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Output Differential Voltage	V <sub>OD</sub>	R <sub>L</sub> = 100 Ω (see figure)	247	355	454	mV
V <sub>DD</sub> Magnitude Change	ΔV <sub>OD</sub>		-50		50	mV
Output High Voltage	V <sub>OH</sub>		1.4	1.6	V	
Output Low Voltage	V <sub>OL</sub>		0.9	1.1	V	
Offset Voltage	V <sub>OS</sub>		1.125	1.2	1.375	V
Offset Magnitude Change	ΔV <sub>OS</sub>		0	3	25	mV
Power-off Leakage	I <sub>OXD</sub>	V <sub>out</sub> = V <sub>DD</sub> or GND V <sub>DD</sub> = 0V		±1	±10	uA
Output Short Circuit Current	I <sub>OSD</sub>			-5.7	-8	mA

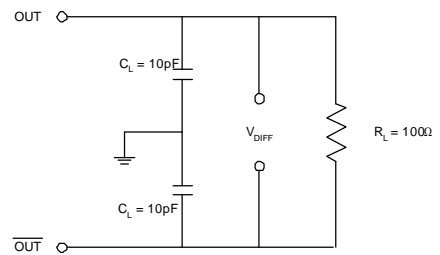
**7.LVDS Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Clock Rise Time	$t_r$	$R_L = 100 \Omega$ $C_L = 10 \text{ pF}$ (see figure)	0.2	0.7	1.0	ns
Differential Clock Fall Time	$t_f$		0.2	0.7	1.0	ns

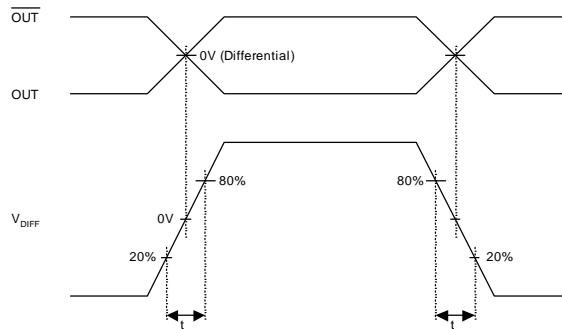
LVDS Levels Test Circuit



LVDS Switching Test Circuit



LVDS Transition Time Waveform

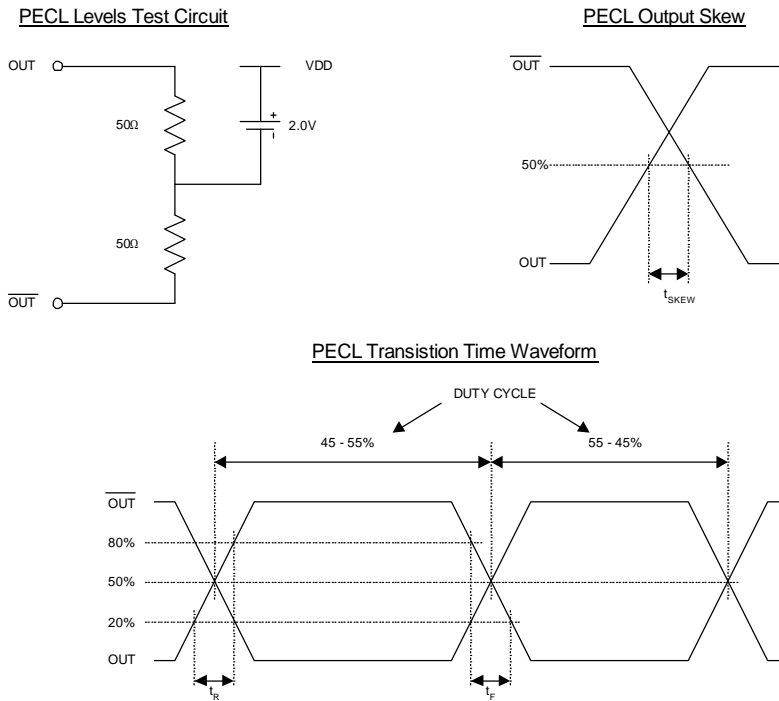


**8. PECL Electrical Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Output High Voltage	$V_{OH}$	$R_L = 50 \Omega$ to $(V_{DD} - 2V)$ (see figure)	$V_{DD} - 1.025$		V
Output Low Voltage	$V_{OL}$			$V_{DD} - 1.620$	V

**9. PECL Switching Characteristics**

PARAMETERS	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Clock Rise Time	$t_r$	@20/80% - PECL		0.6	1.5	ns
Clock Fall Time	$t_f$	@80/20% - PECL		0.5	1.5	ns

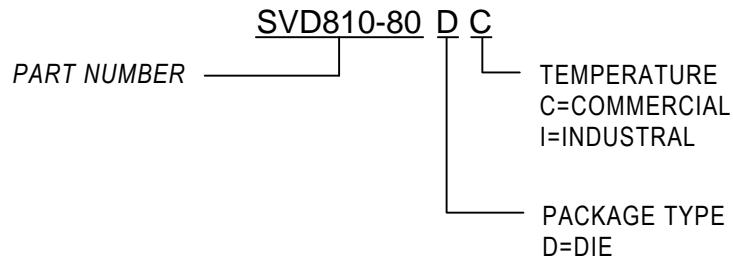


**PAD DESCRIPTIONS**

Pad #	Name	X (μm)	Y (μm)	Description
1	GND	248	109	Ground.
2	GND	361	109	Ground.
3	Optional GND	473	109	Optional Ground.
4	GND	587	109	Ground.
5	GND	702	109	Ground.
6	Reserved	874	109	Reserved for future use.
7	GNDBUF	1042	109	Ground, buffer circuitry.
8	GNDBUF	1171	109	Ground, buffer circuitry.
9	OE_SEL	1400	125	This is the selector input to choose the OE control logic. See the OE SELECTION AND ENABLE table on page 1. Internal pull up.
10	LVDS	1400	259	LVDS output.
11	PECL	1400	476	PECL output.
12	VDDBUF	1400	616	Power supply, buffer circuitry.
13	VDDBUF	1400	716	Power supply, buffer circuitry.
14	PECLB	1400	871	Complementary PECL output.
15	LVDSB	1400	1089	Complementary LVDS output.
16	CMOS	1400	1227	CMOS output.
17	GNDBUF	1389	1365	Ground, buffer circuitry.
18	OUTSEL1	1232	1365	Selector input to choose the selected output type (PECL, LVDS, CMOS). See the OUTPUT SELECTION AND ENABLE table on page 1. Internal pull up.
19	Reserved	1042	1365	Reserved for future use.
20	Not connected	854	1365	Not Connected.
21	VDD	659	1365	Power supply.
22	Optional VDD	559	1365	Optional Power supply.
23	VDD	459	1365	Power supply.
24	VDD	358	1365	Power supply.
25	OUTSEL0	194	1365	Selector input to choose the selected output type (PECL, LVDS, CMOS). See the OUTPUT SELECTION AND ENABLE table on page 1. Internal pull up.
26	XIN	109	1223	Crystal input. See Crystal Specifications on page 3.
27	XOUT	109	1017	Crystal output. See Crystal Specifications on page 3.
28	Not connected	109	858	Not Connected.
29	S2	109	646	Output Divide by Two selector pin, as presented on the OUTPUT FREQUENCY SELECTOR Table on page 1. Internal pull up.
30	OE_CTRL	109	397	Used to enable/disable the output(s). See Output Selection and Enable table on page 1.
31	Not connected	109	181	Not connected.

Note: for optimal Phase Noise performance, it is recommended to bond all optional VDD and GND pads.

**ORDERING INFORMATION**



<u>Order Number</u>	<u>Marking</u>	<u>Package Option</u>
SVD810-80DC	SVD810-80DC	Die – Waffle Pack